



Gallium Nitride 50V, 50W, RF Power Transistor

Description

The STAV25050G2 is a 50-watt, unmatched GaN HEMT, designed for multiple applications with frequencies under 3.0GHz.

The performance is guaranteed for applications operating in the mentioned frequencies

There is no guarantee of performance when this part is used in applications designed

Outside of these frequencies.

•Typical Performance (On Innogrations fixture with device soldered):

$V_{DD} = 48\text{ V}$, $I_{DQ} = 100\text{ mA}$, Pulse Width =20us, Duty Cycle =10%.

Freq (MHz)	Gain@P1dB (dB)	P1dB (dBm)	η_D (%)	P3dB (dBm)	η_D (%)
2400	17.1	48.2	71.3	48.8	74.9
2450	17.5	47.7	71.1	48.6	75.2
2500	17.5	47.3	70.1	48.3	74.4



•Typical Performance (On Innogrations fixture with device soldered):

$V_{DD} = 48\text{ Volts}$, $I_{DQ} = 100\text{ mA}$, CW.

Freq (MHz)	G_P (dB)	P3dB (dBm)	η_D (%)
2400	16.0	48.6	73.2
2450	15.7	48.4	73.8
2500	15.5	48.2	73.5

Applications and Features

- Suitable for 2.4GHz RF heating, Microwave cooking, industry heating application.
- Suitable for wideband power amplifier
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-10 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C



Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=85^\circ\text{C}, T_J=200^\circ\text{C}, \text{DC test}$	$R_{\theta JC}$	2.8	°C /W

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics

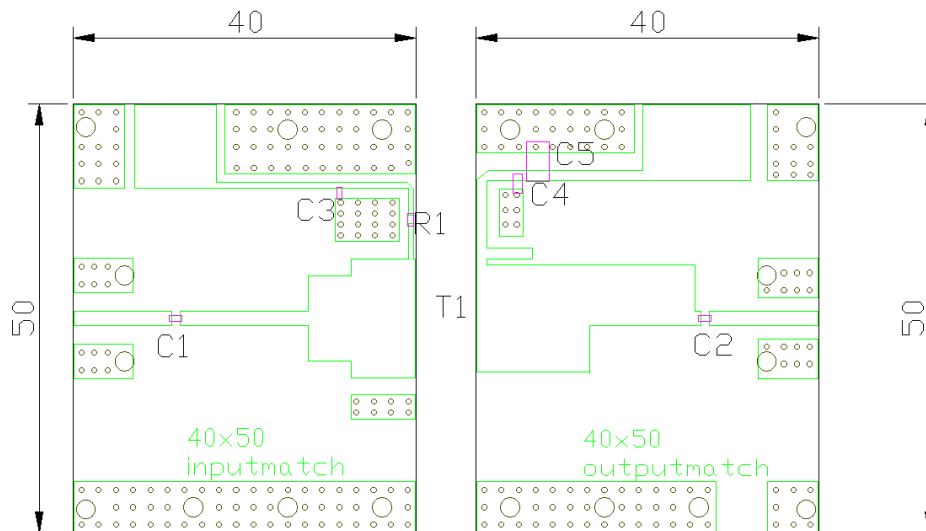
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8\text{V}; I_{DS}=8\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS}=10\text{V}, I_D=8\text{mA}$	$V_{GS(th)}$		-3.8		V
Gate Quiescent Voltage	$V_{DS}=50\text{V}, I_{DS}=100\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.0		V

Functional Tests (In Innogrations Test Fixture, 50 ohm system) : $V_{DD}=50\text{Vdc}, I_{DQ}=100\text{mA}, f=2.45\text{GHz}, \text{Pulsed CW } 20\mu\text{s}/10\%$

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P1dB	G_p		17.5		dB
3dB Compression Point	P_{3dB}		48.6		dBm
Drain Efficiency@P3dB	η_D		75.2		%
Input Return Loss	IRL		-7		dB

Reference Circuit of Test Fixture Assembly Diagram

PCB materials: Roger 4350,30mils, DXF file upon request



Part	Quantity	Description	Part Number	Manufacture
C1,C2,C3, C4	4	100pF High Q Capacitor	251SHS150BSE	TEMEX
C5	1	10uF MLCC	GRM32EC72A10	Murata
R1,	1	10 Ω Power Resistor	ESR03EZPF100	ROHM
T1	1	50W GaN Transistor	STAV25050G2	Innogrations

TYPICAL CHARACTERISTICS

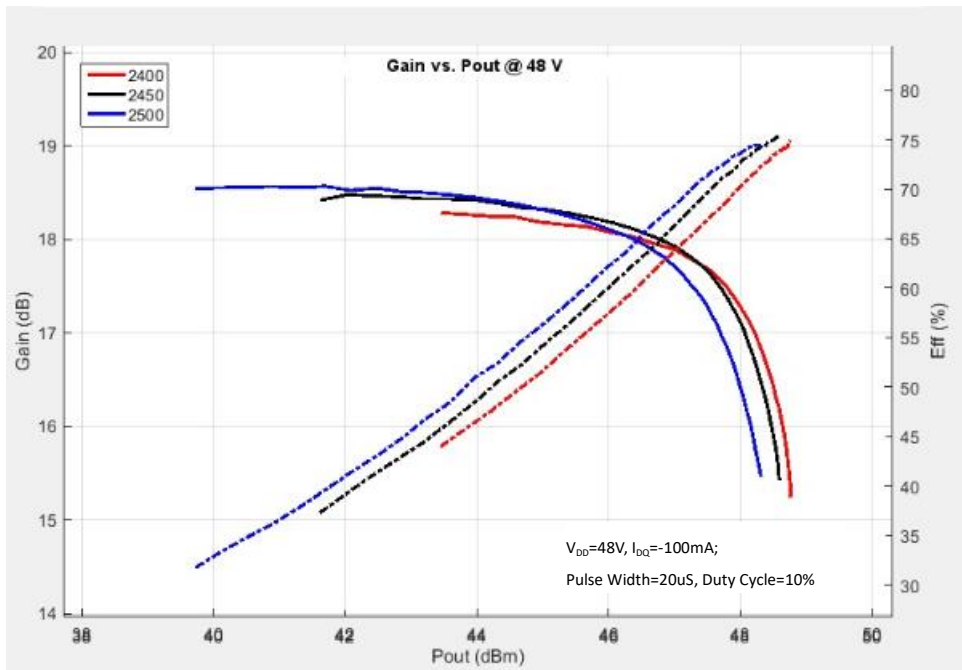


Figure 1. Power gain and drain efficiency as function of Pulse output power



Table 4. Load-Pull Performance:

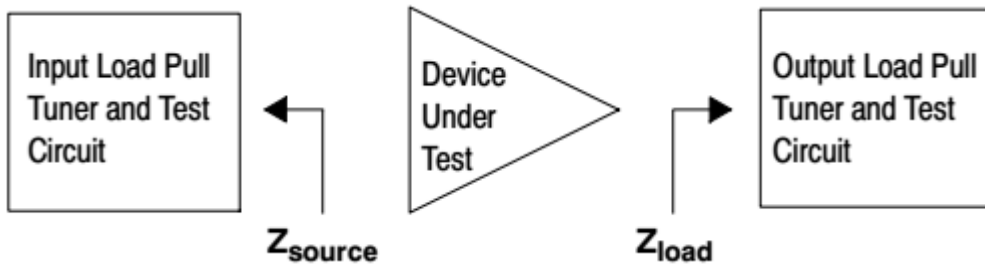
$V_{DD} = 50$ Vdc, $I_{DQ} = 100$ mA, Pulsed CW, Pulse Width=100 us, Duty cycle=10% .

f (MHz)	Tuning Type	Z_{source} (Ω)	P3dB			
			Z_{load} (Ω)	P3dB (dBm)	Gain (dB)	η_o (%)
2400	Max Output Power	1.5-j*3.4	7.8-j*1.2	49.9	15.2	68.8
	Max Drain Efficiency	1.5-j*3.4	4.3+j*3.7	48.0	16.9	77.5
	Trade Off	1.5-j*3.4	6.7+j*2.5	49.4	16.5	75.8
2450	Max Output Power	1.3-j*3.4	7.8-j*1.4	49.8	15.1	68.4
	Max Drain Efficiency	1.3-j*3.4	4.1+j*3.3	47.9	16.9	76.3
	Trade Off	1.3-j*3.4	6.5+j*2.0	49.3	16.3	75.2
2500	Max Output Power	1.0-j*3.5	7.9-j*1.9	49.8	15.1	65.0
	Max Drain Efficiency	1.0-j*3.5	4.1+j*3.0	47.8	17.1	74.8
	Trade Off	1.0-j*3.5	6.5+j*1.6	49.3	16.4	73.4

Note:

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

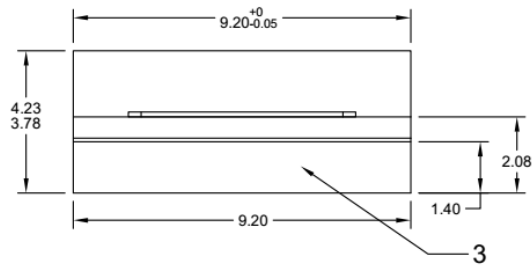
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



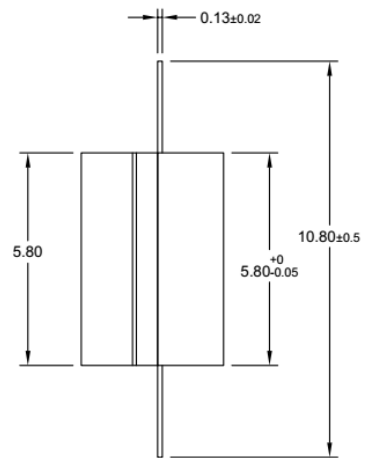
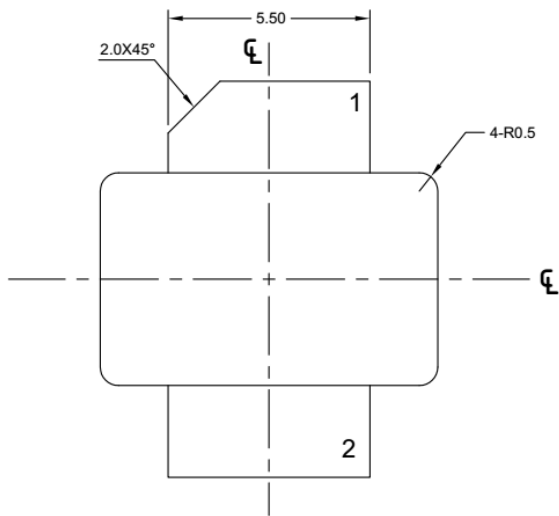


Package Outline

Earless flanged ceramic package; 2 leads



Pin Connection		
1	2	3
Drain	Gate	Source



Unit: mm

Tolerances(unless specified): x.x ±0.25

x.xx ±0.13

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB-2EL-9.2					2018.1.31



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2019/12/25	V1.0	Preliminary Datasheet Creation
2019/12/30	V1.1	Modification on few parameters, and add PCB photo

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