20W,50V HF to Lband Plastic LDMOS Transistor

ITGV10020P3

Description

The ITGV10020P3 is a 20-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 2GHz, in 6*5mm DFN plastic package, supporting surface mounted on PCB through high density grounding vias.

When used at 28V, it can be about 10W with enhanced ruggedness at HF to L band

- Typical Class AB RF Performance in 2 narrow bands (On Innogration fixture with device soldered).

V_{DS}= 50V，I_{DQ}=50mA，V_{GS} =3.5V

FREQ (MHZ)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
400	43.62	23.0	61.2	21.87	44.36	27.3	65.2
450	42.74	18.8	61.3	22.33	43.77	23.8	66.3
500	42.4	17.4	61.3	21.74	43.45	22.1	65.5

V_{DS}= 50V，I_{DQ}=50mA，V_{GS} =3.5V

FREQ (MHZ)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
1470	42.91	19.6	53.5	18.63	43.89	24.5	56.5
1500	42.74	18.8	54.8	18.21	43.72	23.6	57.3
1530	42.55	18.0	54.7	17.81	43.53	22.5	56.6

- Typical Class AB broadband RF Performance (On Innogration fixture with device soldered)

V_{DS}= 28V，I_{DQ}=50mA，V_{GS} =3.5V

Freq (MHz)	Psat (dBm)	Psat (W)	Ids (A)	Pin (dBm)	Gain (dB)	Eff (%)
100	39.89	9.7	0.42	28.49	11.4	82.91
200	40.32	10.8	0.55	28.95	11.37	69.90
300	40.32	10.8	0.69	28.06	12.26	55.72
400	40.35	10.8	0.79	25.39	14.96	49.00
500	40.14	10.3	0.84	29.58	10.56	43.91
600	40.06	10.1	0.85	26.68	13.38	42.60
700	40.28	10.7	0.85	28.93	11.35	44.81
800	40.18	10.4	0.8	29.2	10.98	46.53
900	40.2	10.5	0.79	27.2	13	47.34
1000	40.13	10.3	0.77	26.26	13.87	47.79

Recommended driver: ITEH40001P3

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P band power amplifier
- All 4G/5G cellular application within 0.5 to 1GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	2.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

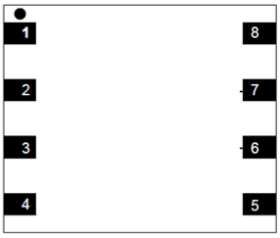
Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 90V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 50V, I_D = 50mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.44	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50Vdc, I_{DQ} = 50mA, f = 1000 MHz

VSWR 10:1 at 20W pulse CW Output Power	No Device Degradation

Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
1,2,3,4	RF IN/VGS	Gate Bias/RF Input
5,6, 7,8	RF OUT /VDS	RF Output, Drain Bias
Backside metal	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

400-500MHz 50V application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

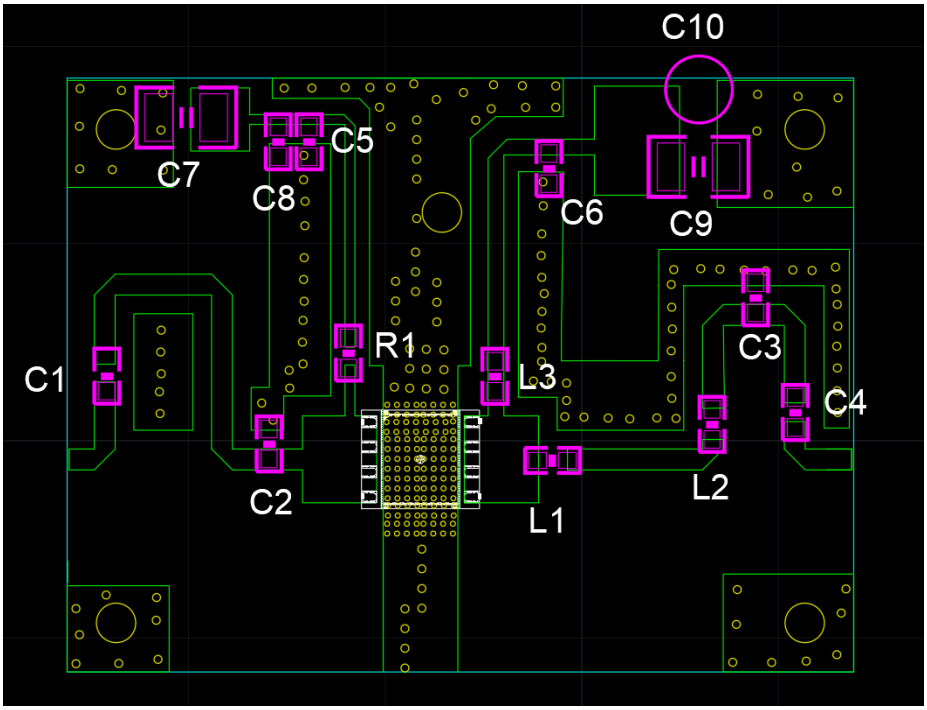


Figure 2. Test Circuit Component Layout

Component	Value	Quantity
U1	ITGV10020P3	1
C1、C4、C5、C6	330pF	4
C2、C3	1.8pF	2
C7、C9	10uF/63V	2
C8	10uF/16V	1
C10	470uF/63V	1
R1	10Ω	1
L1	6.8nH	1
L2	5.6nH	1
L3	47nH	1

TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output

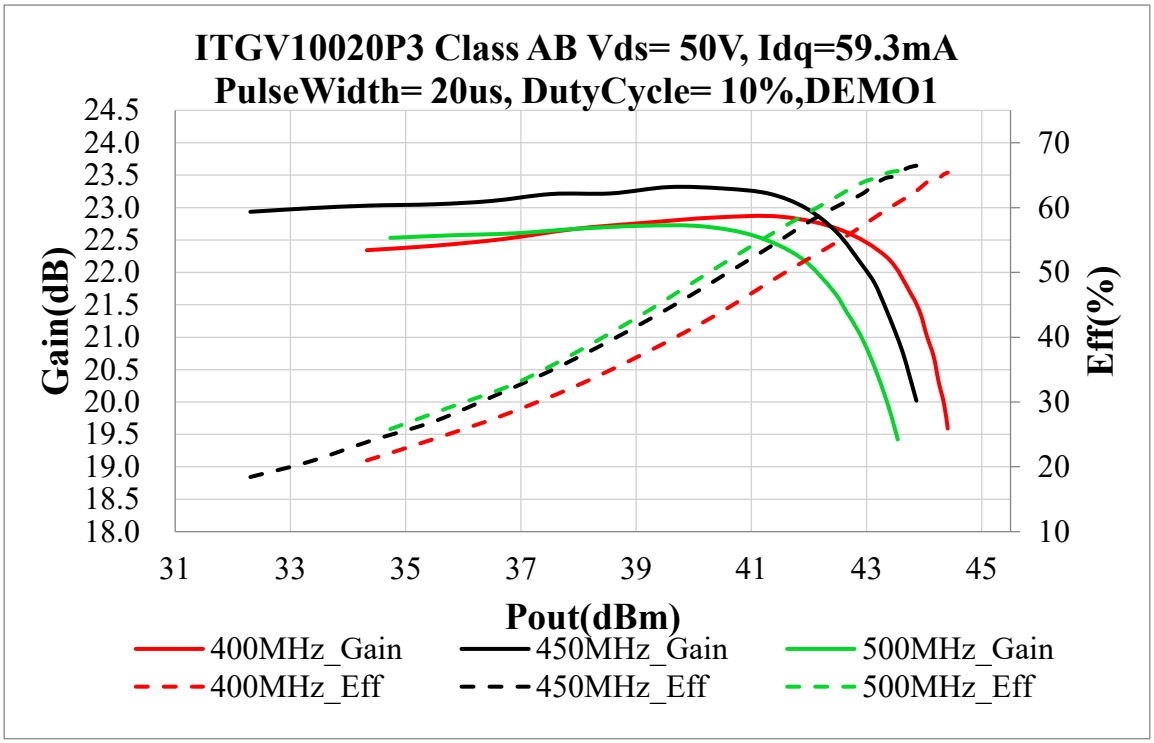
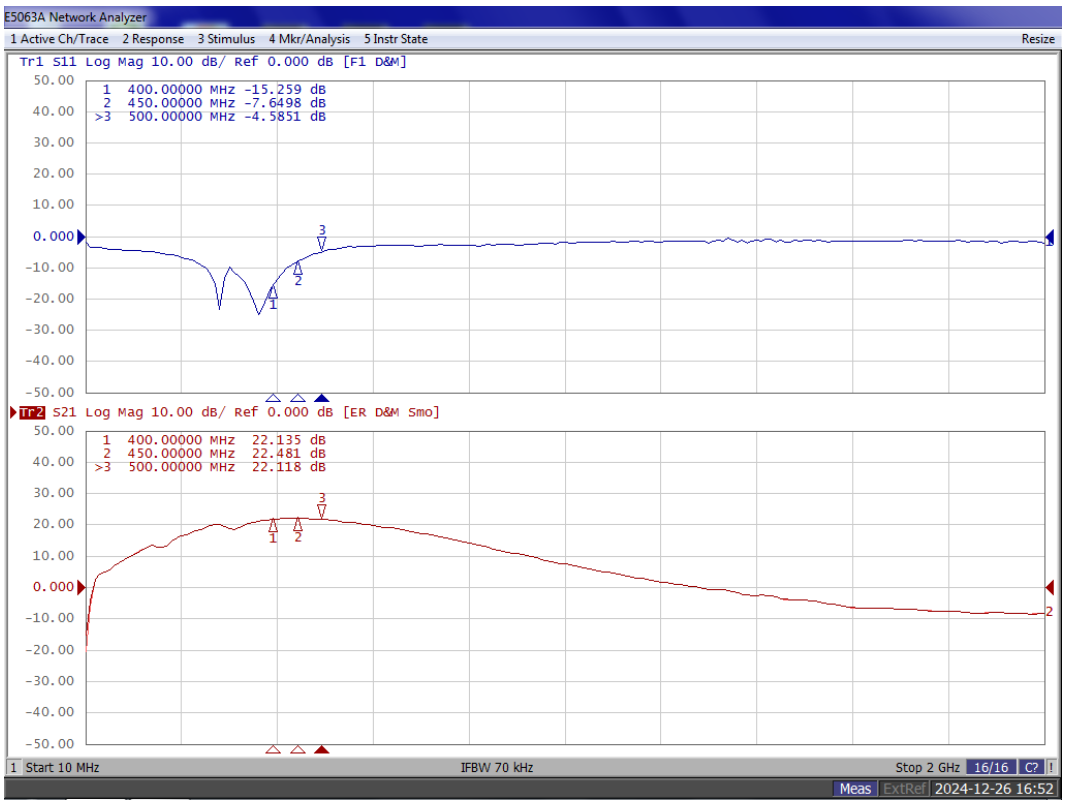


Figure 4.Network analyzer output S11/S21



1500MHz 50V application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

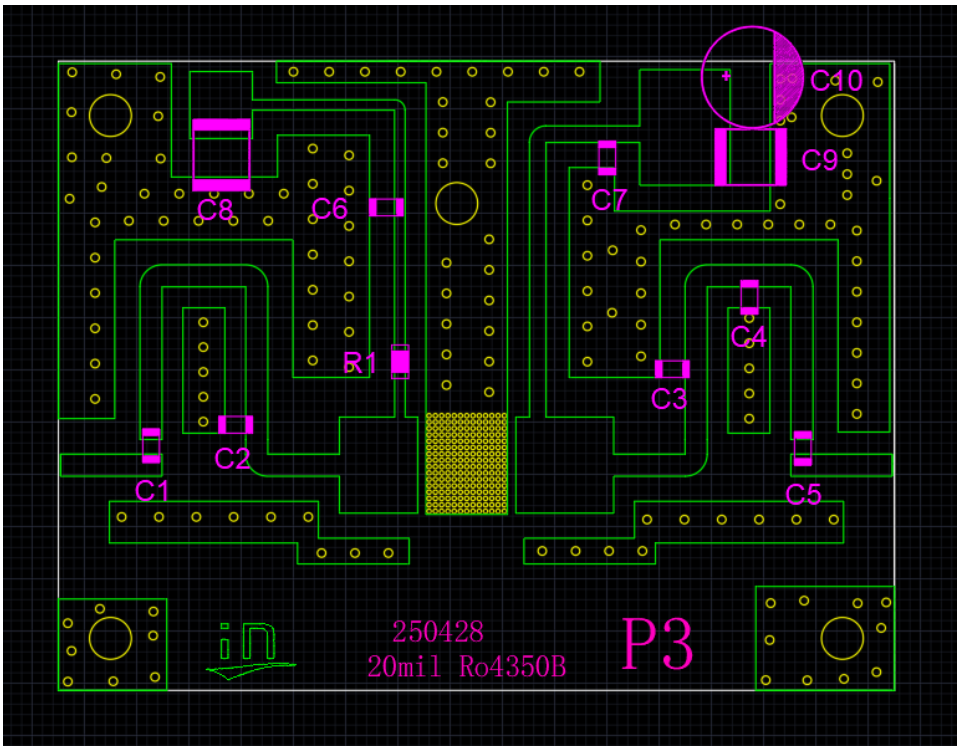


Figure 5. Test Circuit Component Layout

Component	Value	Quantity
U1	ITGV10020P3	1
C1、C5、C6、C7	20pF	4
C2	4.3pF	1
C3	3.3pF	1
C4	1.5pF	1
C8、C9	10uF/63V	2
C10	470uF/63V	1
R1	10Ω	1

TYPICAL CHARACTERISTICS

Figure 6. Power Gain and Drain Efficiency as function of Power Output

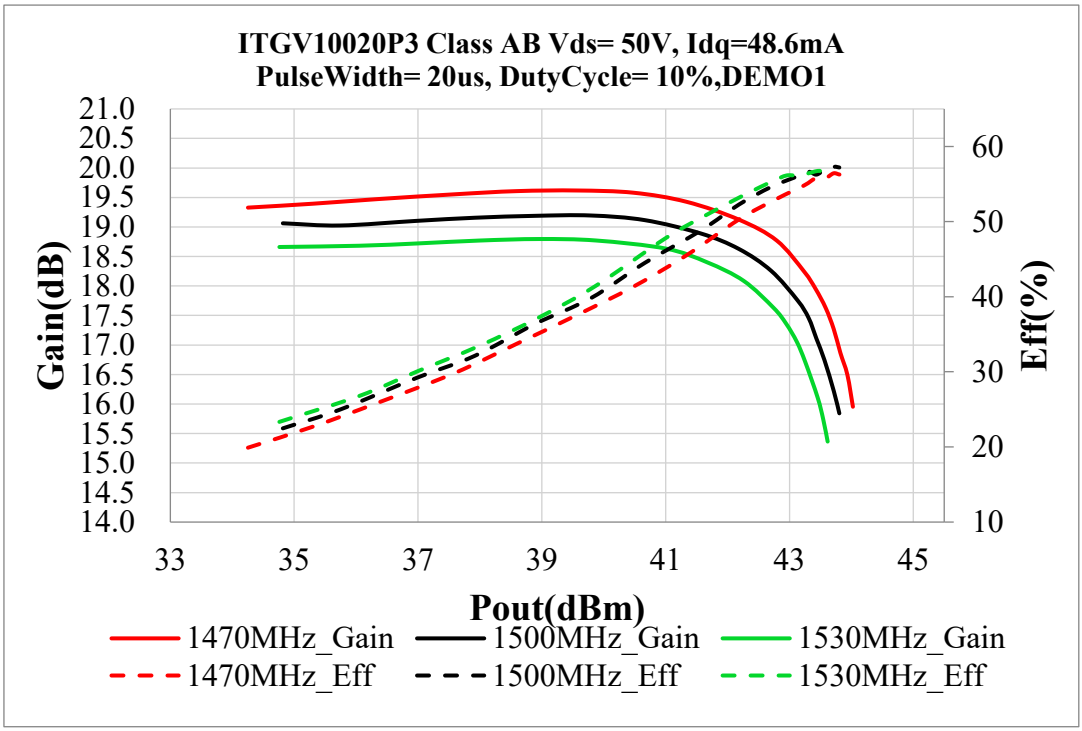
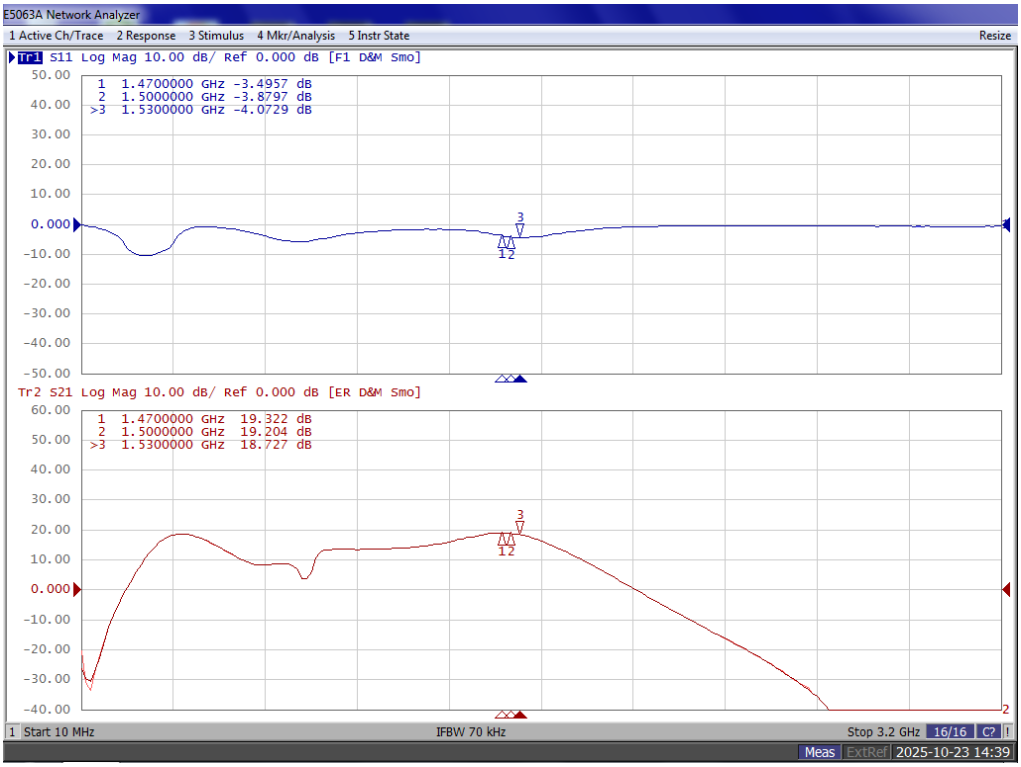


Figure 7.Network analyzer output S11/S21



100-1000MHz 28V application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

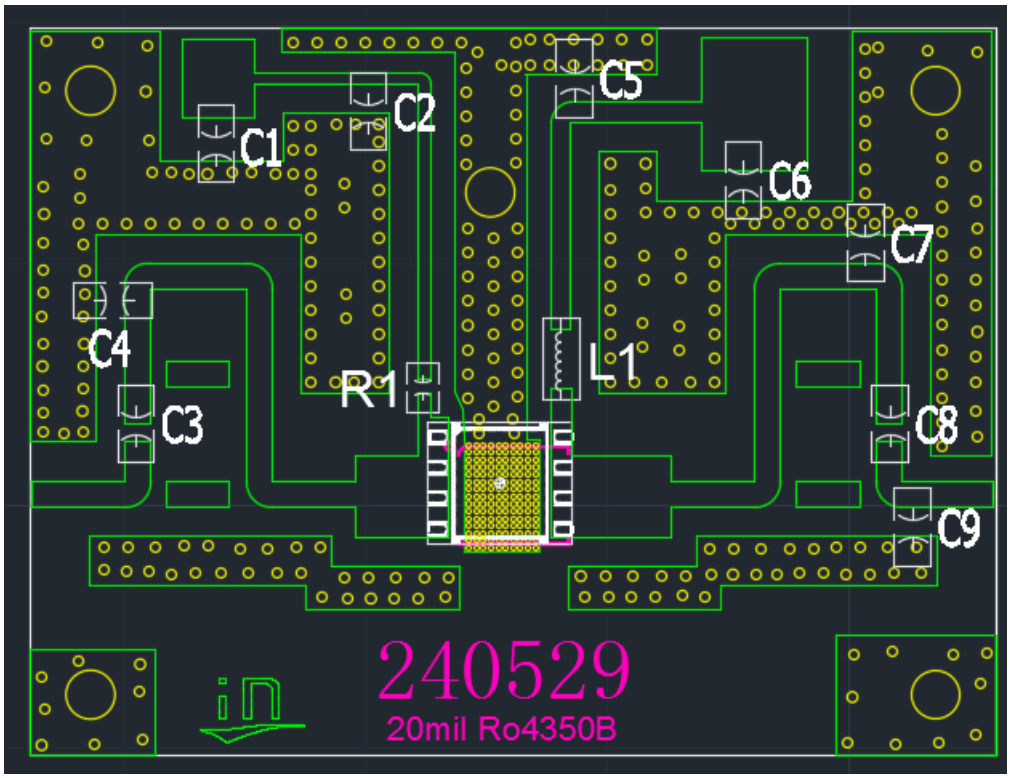
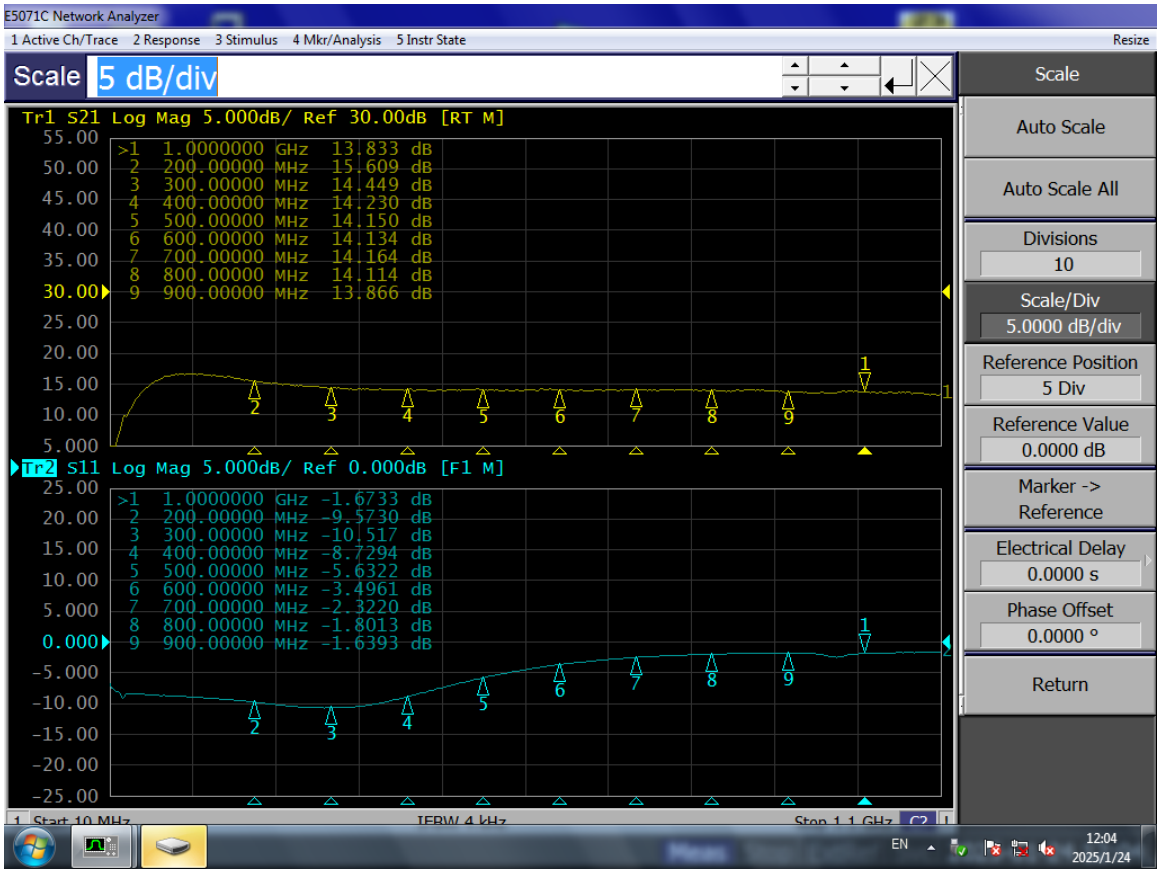


Figure 8. Test Circuit Component Layout

C1,C6	10uF/1210	/
C2,C5	1000pF/MQ40-0805	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
C3	820pF/MQ301111	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
C4	1.8pF/MQ40-0805	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
C7	3pF/MQ40-0805	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
C8	560pF/MQ301111	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
C9	0.5pF/MQ40-0805	BEIJING YUANLU HONGYUAN ELECTRONICTECHNOLOGY CO., LTD
R1	22Ω/0805	/
L1	160nH/1812-1.2A	/

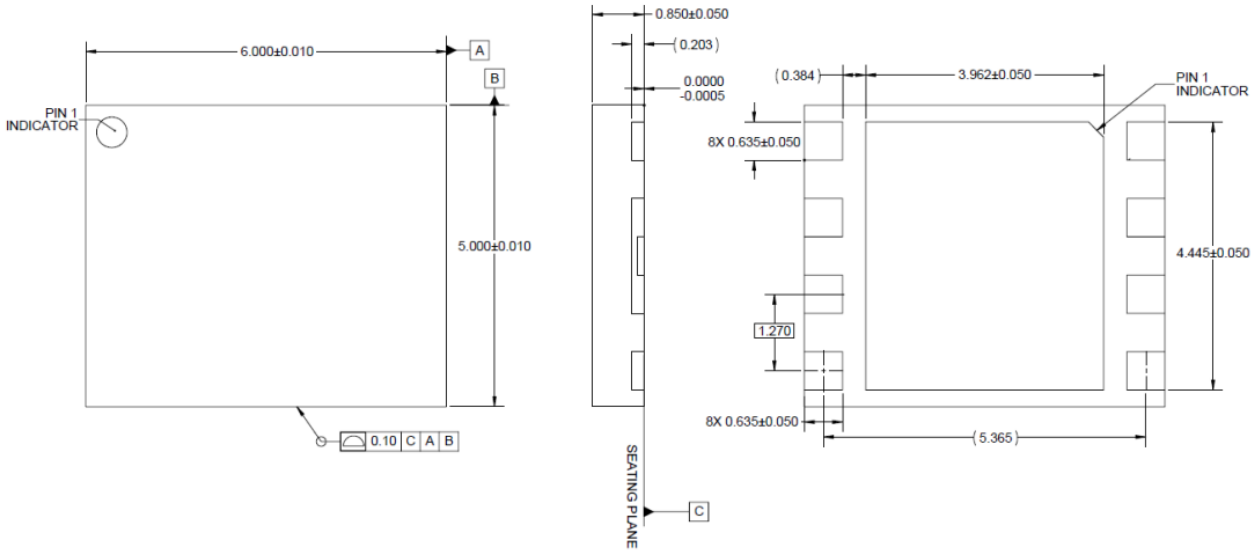
TYPICAL CHARACTERISTICS

Figure 9.Network analyzer output S11/S21



Package

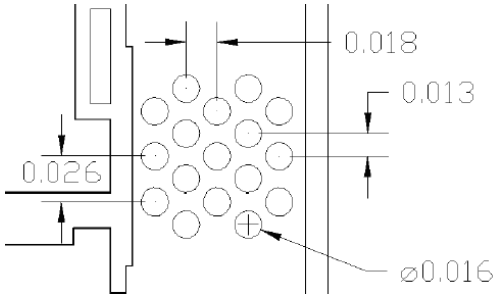
6*5 DFN Package



Notes:

1. All dimensions are in mm. Otherwise noted, the tolerance is ±0.1 mm.
2. Package leads are gold plated.
3. Part is mold encapsulated.

Recommended vias layout: (all in inches)



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2024/12/26	**Rev 1.0**	**Preliminary Datasheet**
2025/2/9	**Rev 1.1**	Add 0.1-1G broadband application data
2025/10/24	**Rev 2.0**	Update the upper frequency limits to 2GHz

Application data based on ZYX-24-72/73, SJJ-25-01, ZYX-25-45

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