

# STBV07750RC2 GaN TRANSISTOR

Document Number: STBV07750RC2  
Preliminary Datasheet V1.0

## 750W ,50V UHF/VHF CW RF Power Transistor

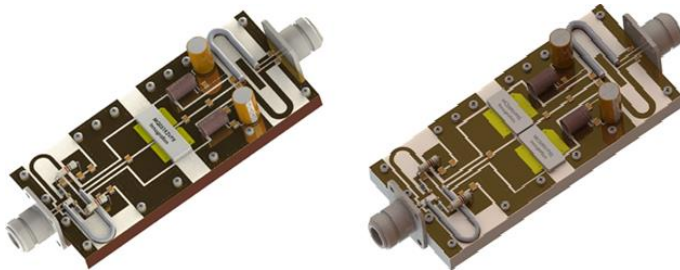
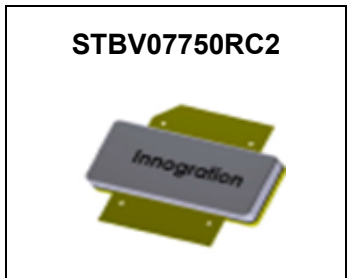
### Description

The STBV07750RC2 itself is a 750-watt capable, high performance, internal match, single ended GaN HEMT transistor, idea for RF Energy and ISM application at fixed frequency point or very narrow band below 700MHz, typically for 650MHz or 433MHz applications.

There is no guarantee of performance when this part is used outside of stated frequencies.

**It is recommended to use paired STBV07750RC2 to enable >1300W designed for ISM application. Compared to similar power level but in single dual-path packaged device, it offers better thermal management and easier maintenance.**

Demonstration of paired STBV07750RC2(right) Vs single dual-path device(left) at 650MHz



- Typical performance(on 650MHz narrow band application board with **STBV07750RC2** devices soldered)

$V_{DS}=50V, V_{GS}=-4.2V, CW,$

VDS (V)	Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
48	650	57.81	603.5	77.5	18.32	58.46	702.1	81.3
50	650	58.23	665.5	77.5	18.31	58.82	762.4	81.2

### Applications

- P band amplifier
- UHF/VHF PA

### Important Note: Proper Biasing Sequence for GaN HEMT Transistors

#### Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically  $-5 V$
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

#### Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically  $-5 V$
3. Reduce VDS down to 0 V
4. Turn off VGS

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	+200	Vdc
Gate--Source Voltage	$V_{GS}$	-8 to +0.5	Vdc
Operating Voltage	$V_{DD}$	55	Vdc
Maximum gate current	$I_{GS}$	100	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}C$
Case Operating Temperature	$T_C$	+150	$^{\circ}C$

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Operating Junction Temperature	$T_J$	+225	°C
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**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C = 25^\circ\text{C}$ , at $P_d = 190\text{W}$	$R_{\theta JC}$	0.6	°C /W

**Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)**

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$ ; $I_{DS} = 108\text{mA}$	$V_{DSS}$		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$ , $I_D = 108\text{mA}$	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$ , $I_{DS} = 500\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		-3.4		V

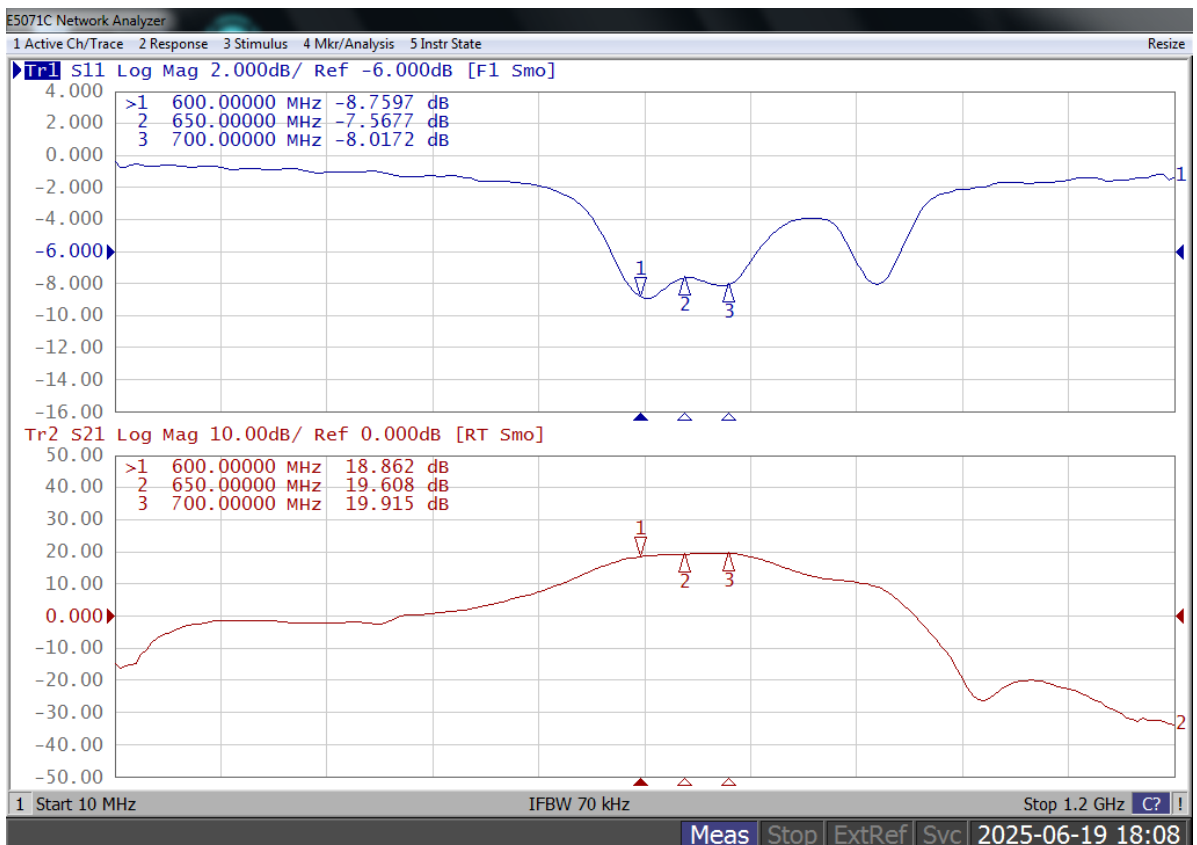
Ruggedness Characteristics in Paired configurations

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	0.7GHz, $P_{out} = 750\text{W}$ pulse CW All phase, No device damages	VSWR		5:1		

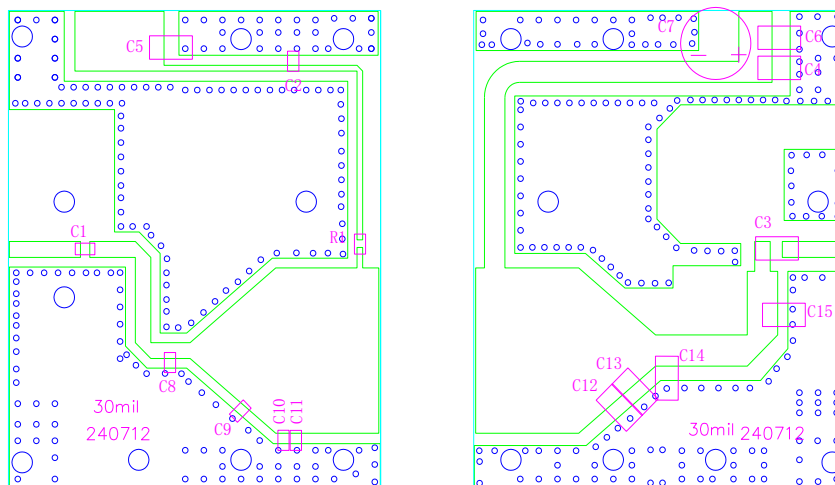
## TYPICAL CHARACTERISTICS

STBV07750RC2 at 650MHz

Figure 1: Network analyzer output S11/S21  $V_{ds} = 50\text{V}$ ,  $I_{dq} = 600\text{mA}$ ,  $P_{in} = 0\text{dBm}$



## Reference Circuit of Test Fixture

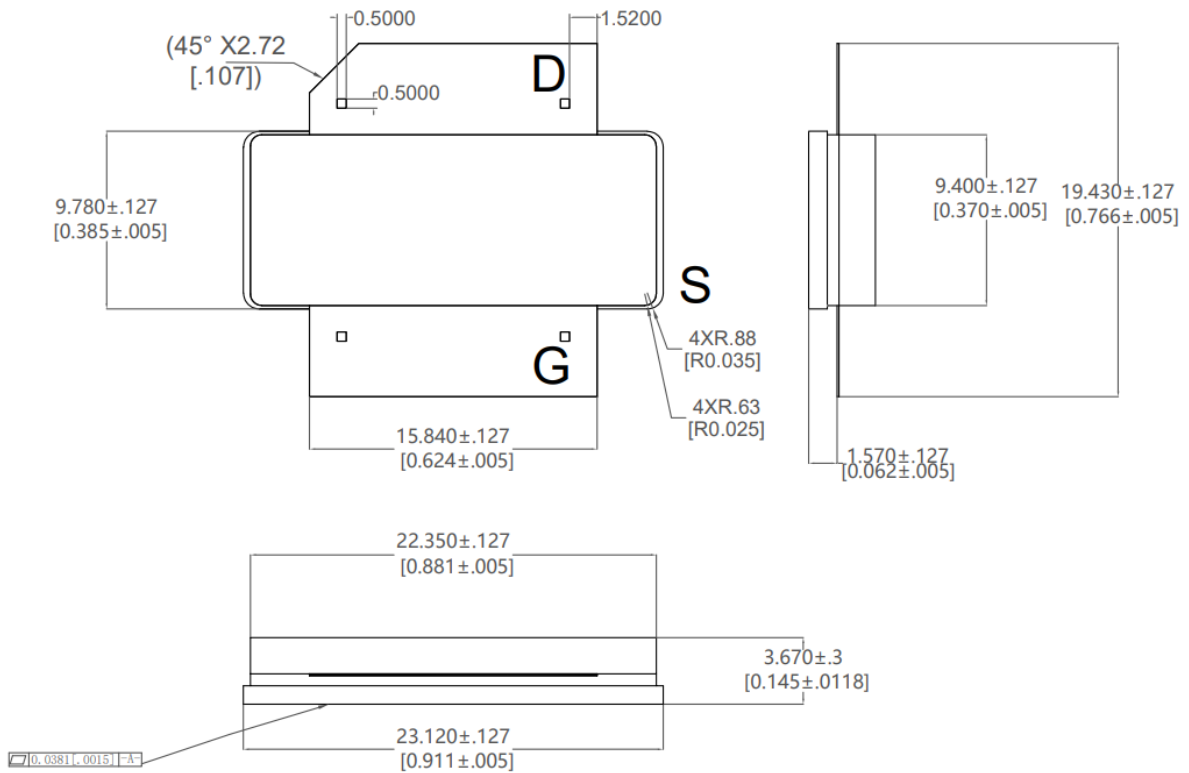


Designator	Footprint	Comment	Quantity
C1	0603/0805	4.7pF	1
C2	0603/0805	82pF	1
C3, C4	1210	82pF	2
C5, C6	1210	10 uF/100V	2
C7		1000 uF/63V	1
C8, C10, C11	0603/0805	15 pF	3
C9	0603/0805	10 pF	1
C12, C13, C14, C15	1210	10 pF	4
R1	0603	10 $\Omega$	1

## Package Outline

Flangeless ceramic package;

### INP-688-2-EL (C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

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## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/6/20	Rev 1.0	Preliminary datasheet

Application data based on TC-25-17

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