



## 20W,28V Plastic RF LDMOS Transistor

**ITCH20020P3**

### Description

The ITCH20020P3 is a 20-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 2.0GHz, in 6\*5mm DFN plastic package, supporting surface mounted on PCB through high density grounding vias.

•Typical **UHF** Class AB RF Performance (On Innegration fixture with device soldered).

VDS=28V, IDQ=100mA Pulsed CW: 100 us width, 20% duty cycle.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
700	44.15	26.0	69.5	18.7	44.92	31.1	72.7
800	44.03	25.3	65.4	19.79	44.98	31.5	70.3
900	43.88	24.5	64.3	20.08	44.95	31.3	69.4
960	43.69	23.4	65.1	19.45	44.82	30.4	70.3

Typical **L band** Class AB RF Performance (On Innegration fixture with device soldered).

VDS=28V, IDQ=100mA Pulsed CW: 100 us width, 20% duty cycle.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
1400	43.79	23.92	58.27	16.57	44.72	29.68	60.79
1500	43.42	21.99	57.28	16.49	44.60	28.85	61.11
1600	42.88	19.39	56.91	16.06	44.04	25.34	59.68

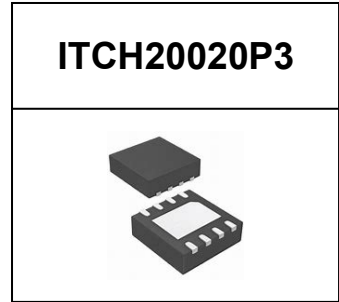
VDS=28V, IDQ=100mA Pulsed CW: 100 us width, 20% duty cycle.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
1800	44.53	28.4	51.9	13.91	45.3	33.9	53.6
1900	44.23	26.5	54.4	14.11	45.06	32.1	56.1
2000	43.51	22.4	54.9	13.32	44.28	26.8	55.5

VDS=28V, IDQ=100mA CW

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
1300	42.91	19.5	54.8	14.07	43.78	23.9	57.0
1400	43.61	23.0	49.9	14.13	44.47	28.0	52.1
1500	44.03	25.3	49.5	14.91	44.84	30.5	51.8
1600	44.02	25.3	48.7	15.39	44.94	31.2	51.3
1700	44.11	25.7	51.7	15.12	45.06	32.1	54.6
1800	44.13	25.9	57.3	14.28	44.98	31.5	59.2
1900	43.48	22.3	56.7	13.92	44.25	26.6	57.3

**Note: High linear tuning result for each band upon request**





**Features**

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

**Suitable Applications**

- Broadcast and Industrial, Scientific and Medical applications in the frequency range from HF to 2.0GHz
- All 4G/5G cellular application below 2.0GHz

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DS}$	+65	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+28	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_J$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ\text{C}$ , $P_{out} = 20\text{W}$ 2GHz	$R_{\theta JC}$	0.9	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

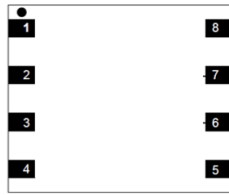
Characteristic	Symbol	Min	Typ	Max	Unit
Drain-Source Voltage $V_{GS} = 0$ , $I_{DS} = 100\mu\text{A}$	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{V}$ , $V_{GS} = 0\text{V}$ )	$I_{DSS}$	---	---	1	$\mu\text{A}$
Gate--Source Leakage Current ( $V_{GS} = 11\text{V}$ , $V_{DS} = 0\text{V}$ )	$I_{GSS}$	---	---	1	$\mu\text{A}$
Gate Threshold Voltage ( $V_{DS} = 28\text{V}$ , $I_D = 600\mu\text{A}$ )	$V_{GS(th)}$	---	2	---	V
Gate Quiescent Voltage ( $V_{DD} = 28\text{V}$ , $I_D = 100\text{mA}$ , Measured in Functional Test)	$V_{GS(Q)}$	---	2.4	---	V

**Load Mismatch (In Innegration Test Fixture, 50 ohm system):**  $V_{DD} = 28\text{Vdc}$ ,  $I_{DQ} = 100\text{mA}$ ,  $f = 2100\text{MHz}$

VSWR 10:1 at 10W pulse CW Output Power	No Device Degradation
--	-----------------------



### Pin Configuration and Description(Top view)

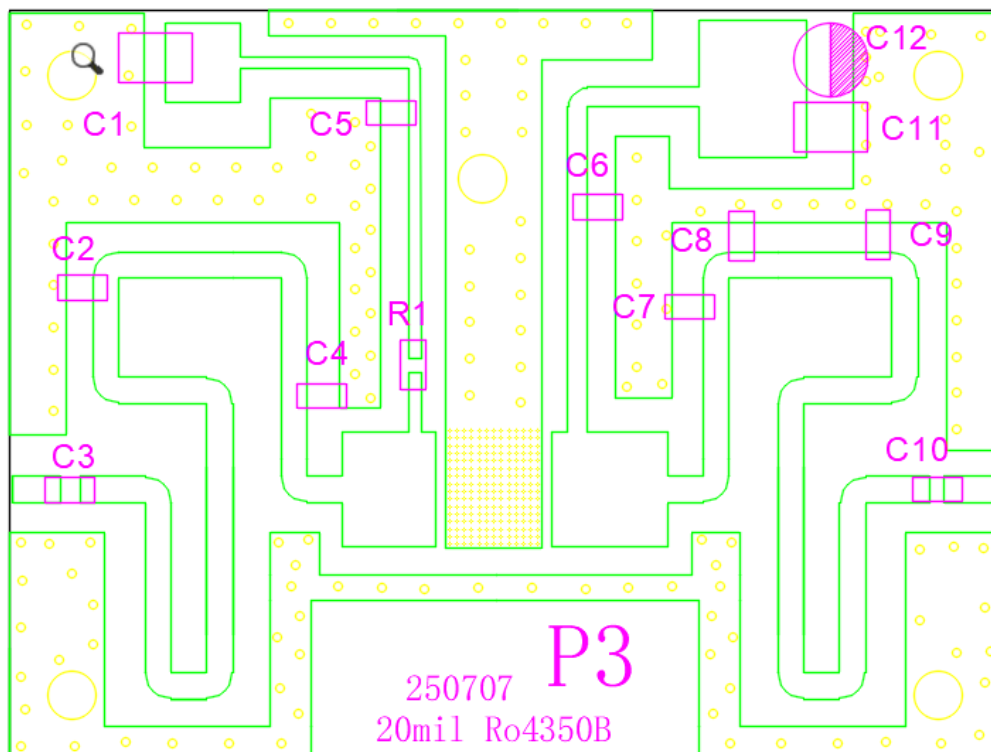


Pin No.	Symbol	Description
1,2,3,4	RF IN/VGS	Gate Bias/RF Input
5,6, 7,8	RF OUT /VDS	RF Output, Drain Bias
Backside metal	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

## 700-960MHz

### Reference Circuit of Test Fixture Assembly Diagram

20mils RO4350B



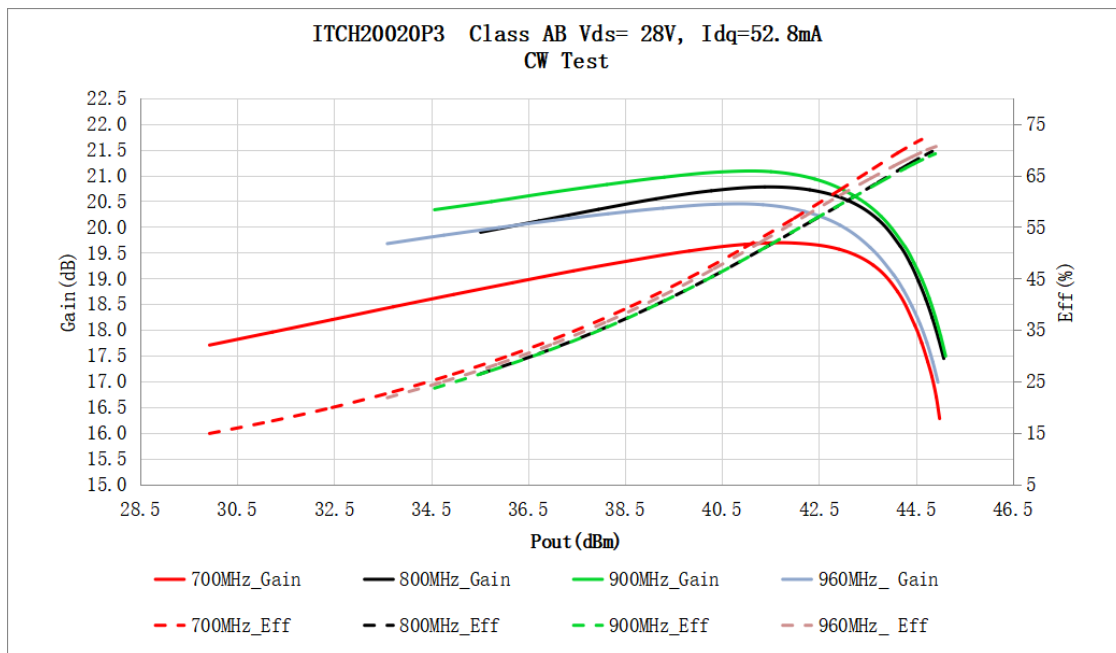


Test Circuit Component Layout

Component	Value	Footprint	Quantity
C1,C11	10uF/63V	1210	2
C2	4.7pF	0603	1
C3,C5,C6,C10	68pF	0603	4
C4	8.2pF	0603	1
C7	1.8pF	0603	1
C8,C9	2.2pF	0603	2
C12	470Uf/63V		1
R1	10 ohm	0603	1
U1	ITCH20020P3	DFN6*5	1

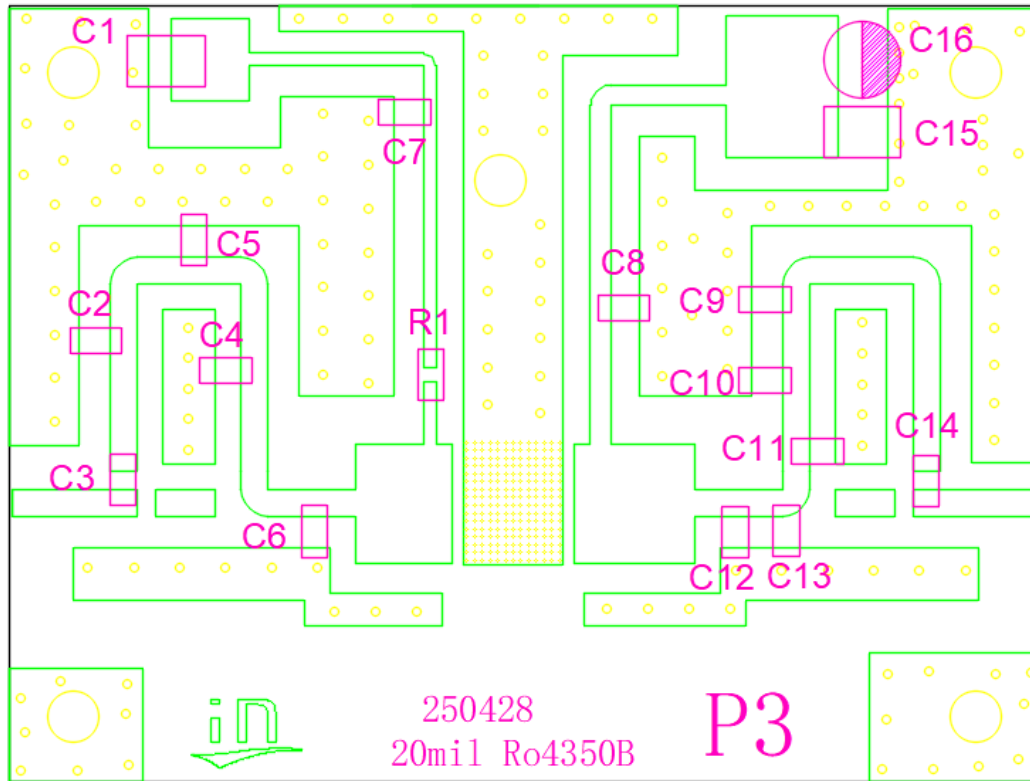
TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output



## 1400-1600MHz

### Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

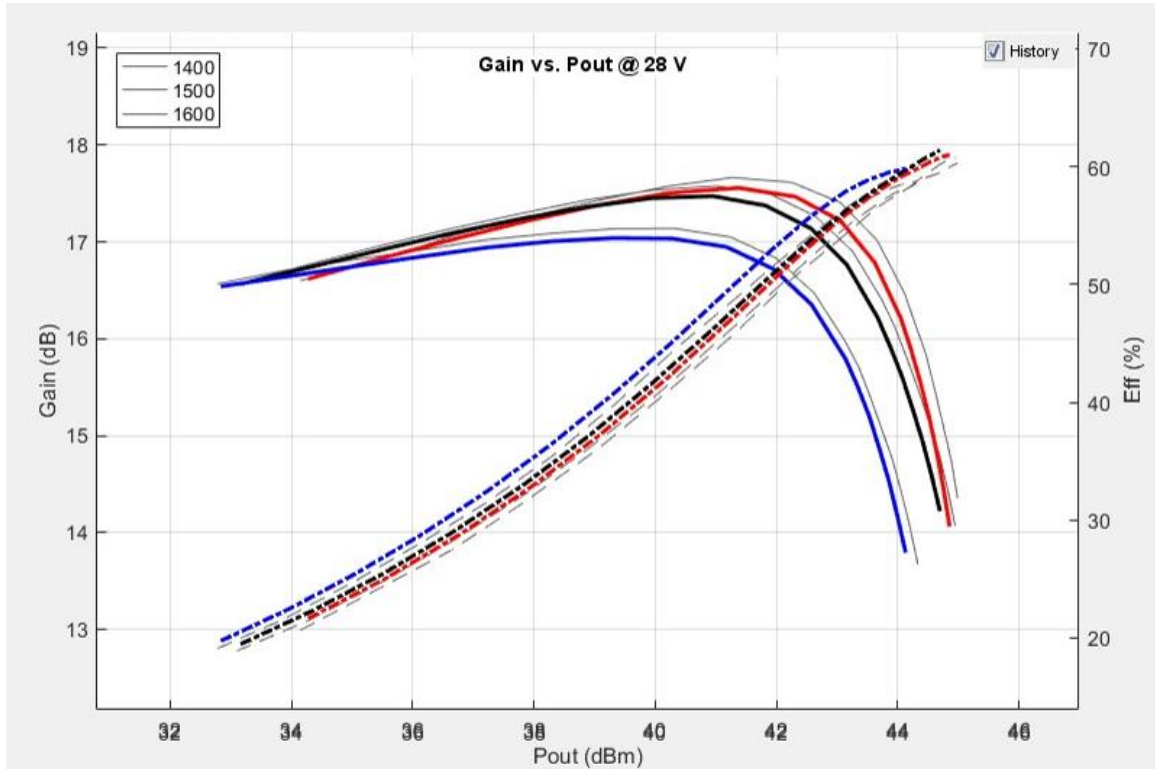


Test Circuit Component Layout

Component	Value	Footprint	Quantity
C1,C15	10uF/63V	1210	2
C2	0.3pF	0603	1
C3,C7,C8,C14	22pF	0603	4
C4	1pF	0603	1
C5,C11	1.8pF	0603	2
C6	7.5pF	0805	1
C9	1.6pF	0805	1
C10	0.2pF	0603	1
C12	2.2pF	0603	1
C13	0.5pF	0603	1
C12	470Uf/63V		1
R1	10 ohm	0603	1
U1	ITCH20020P3	DFN6*5	1

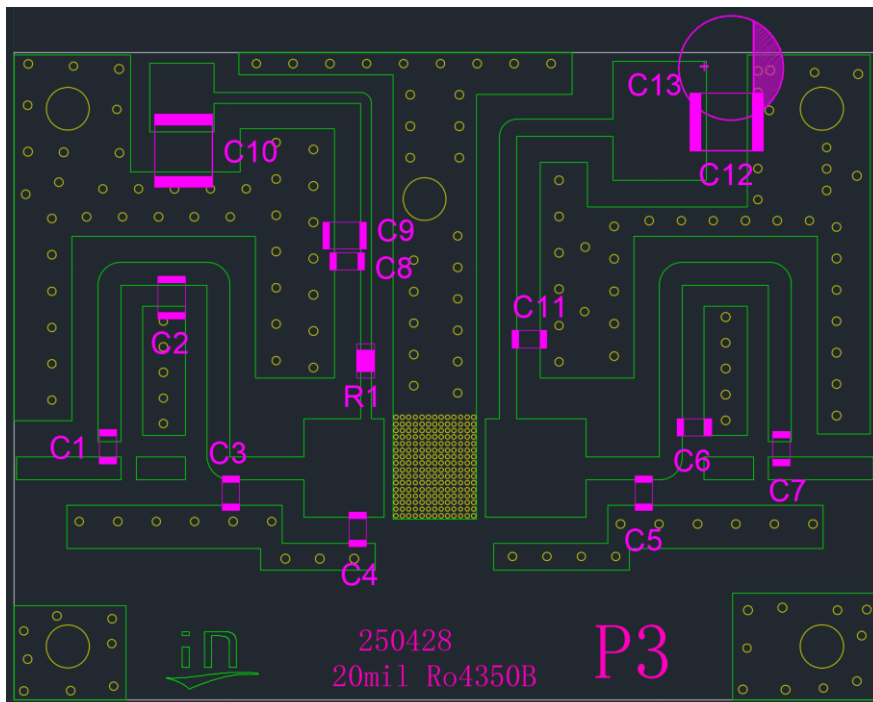
**TYPICAL CHARACTERISTICS**

Figure 3. Power Gain and Drain Efficiency as function of Power Output



**1800-2000MHz**

Reference Circuit of Test Fixture Assembly Diagram  
20mils RO4350B



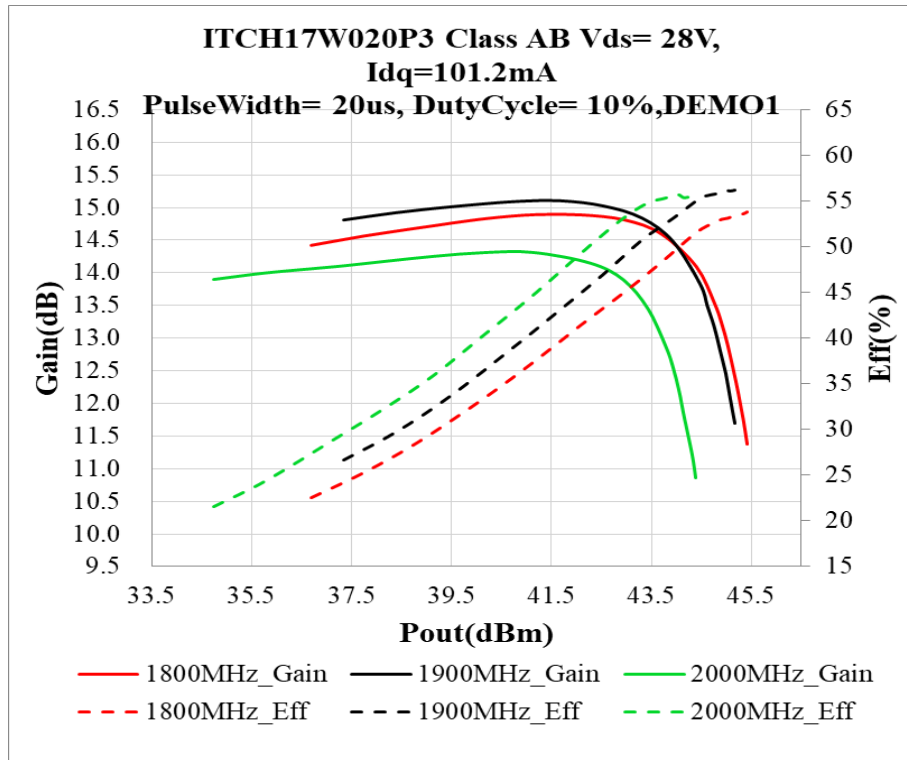


Test Circuit Component Layout

Component	Value	Footprint	Quantity
C1	0603	10 pF	1
C2	0805	0.8 pF	1
C3	0603	3.6 pF	1
C4	0603	4.3 pF	1
C5	0603	2.4 pF	1
C6	0603	1.2 pF	1
C7,C8,C11	0603	20 pF	3
C9	0805	10 nF	1
C10,C12	1210	10 uF/63V	2
C13	/	470 uF	1
R1	0603	10 ohm	1
U1	P3	ITCH20020P3	1

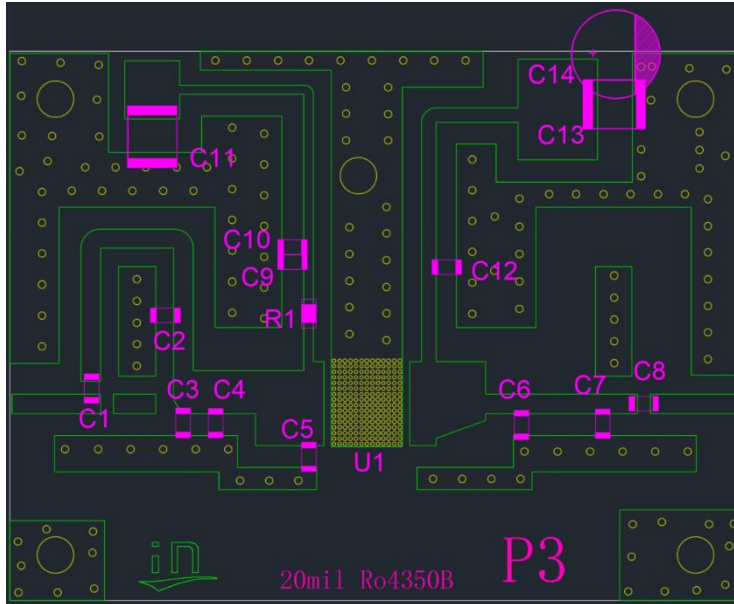
TYPICAL CHARACTERISTICS

Figure 4. Power Gain and Drain Efficiency as function of Power Output



## 1300-1900MHz

### Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B



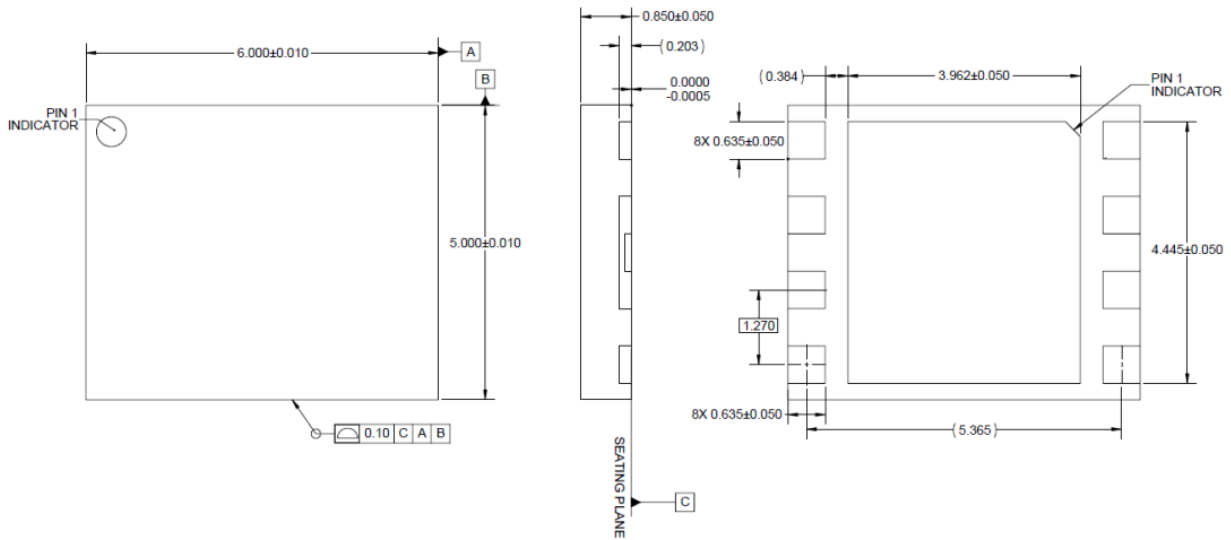
Test Circuit Component Layout

Reference	Footprint	Value	Quantity
C1,C8	0603	15 pF	2
C2	0603	2.7 pF	1
C3	0603	2 pF	1
C4	0603	3.3 pF	1
C5	0603	5.6 pF	1
C6	0603	2.4 pF	1
C7	0603	1.8 pF	1
C9,C12	0603	12 pF	2
C10	0603/0805	10 nF	1
C11,C13	1210	10 uF/63V	2
C14	\	470 uF/63V	1
R1	0603	10 ohm	1
U1	P3	ITCH20020P3	1



**Package Outline**

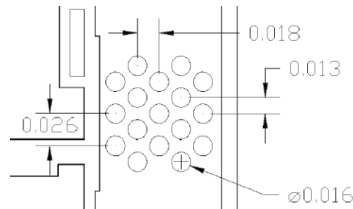
**6\*5 DFN Package**



**Notes:**

1. All dimensions are in mm. Otherwise noted, the tolerance is  $\pm 0.1$  mm.
2. Package leads are gold plated.
3. Part is mold encapsulated.

**Recommended via layout: (all in inches)**



**Revision history**

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/8/12	Rev 1.0	Preliminary Datasheet
2025/12/24	Rev 1.1	Add 1.3-1.9G data

**Application data based on CWZ-25-10/12/15**

**Disclaimers**

Specifications are subject to change without notice. Innegration believes the information contained within this data sheet to be accurate and reliable. However, no responsibility is assumed by Innegration for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Innegration. Innegration makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose. "Typical" parameters are the average values expected by Innegration in large quantities and are provided for information purposes only. These values can and do vary in different applications and actual performance can vary over time. All operating parameters should be validated by customer's technical experts for each application. Innegration products are not designed, intended or authorized for use as components in applications intended for surgical implant into the body or to support or sustain life, in applications in which the failure of the Innegration product could result in personal injury or death or in applications for planning, construction, maintenance or direct operation of a nuclear facility. For any concerns or questions related to terms or conditions, pls check with Innegration and authorized distributors

Copyright © by Innegration (Suzhou) Co.,Ltd.