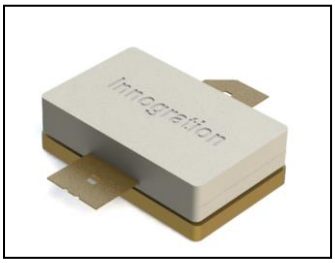
100W,50V Plastic RF LDMOS Transistor



Description

The ITGV10100T2C is a 100-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 1.5GHz. **It is based on air cavity plastic package named as T2C with outline highly compatible as TO270 from other suppliers**

- Typical Class AB RF Performance (On Innogration fixture with device soldered).

Vds=50V, Idq=200mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1400	50.37	108.93	59.89	18.06	51.0	126	60

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- RF power amplifiers for CW applications
- Industrial, scientific and medical applications
- Broadcast transmitter applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	1.1	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current	I_{DSS}	——	——	1	μA

(V_{DS} = 90V, V_{GS} = 0 V)					
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 50V, I_D = 200mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50Vdc, I_{DQ} = 200mA, f = 1500 MHz

VSWR 10:1 at 100W pulse CW Output Power	No Device Degradation

1400MHz application board

Reference Circuit of Test Fixture Assembly Diagram
30mils RO4350B

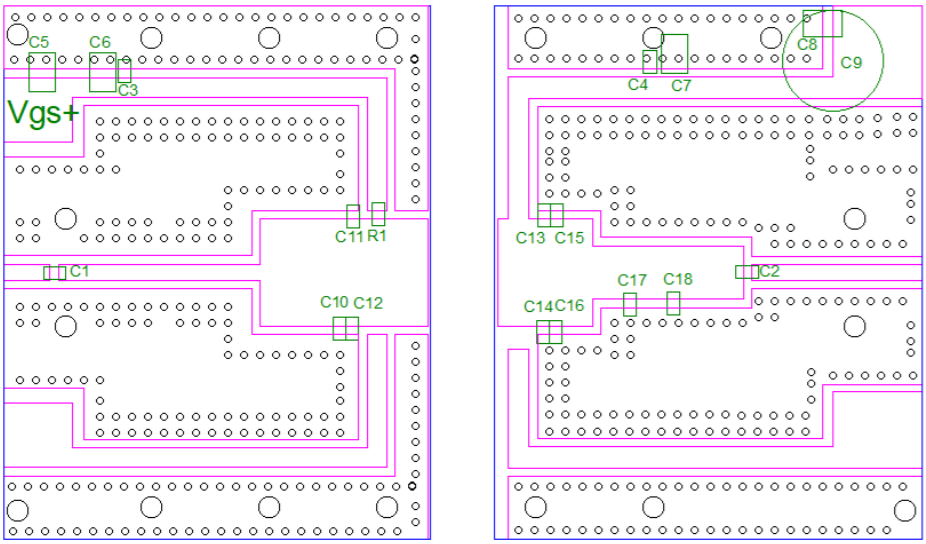


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Part	Quantity	Description	Part Number	Manufacture
C1	1	3.9pFHigh Q Capacitor	251SHS3R9BSE	TEMEX
C2,C3,C4	3	30pFHigh Q Capacitor	251SHS301BSE	TEMEX
C10	1	2.7pFHigh Q Capacitor	251SHS2R7BSE	TEMEX
C11,C12	2	3.3pFHigh Q Capacitor	251SHS3R3BSE	TEMEX
C13,C14	2	4.7pFHigh Q Capacitor	251SHS4R7BSE	TEMEX
C15,C16	2	0.3pFHigh Q Capacitor	251SHS0R3BSE	TEMEX
C17	1	3.9pFHigh Q Capacitor	251SHS3R9BSE	TEMEX
C18	1	0.2pFHigh Q Capacitor	251SHS0R2BSE	TEMEX
R1	1	10Ω Power Resistor	ESR03EZPF100	ROHM
C5,C6,C7,C8	4	10uF MLCC	GRM32EC72A106ME05	Murata
C9	1	470ufCapacito	/	/

TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output)

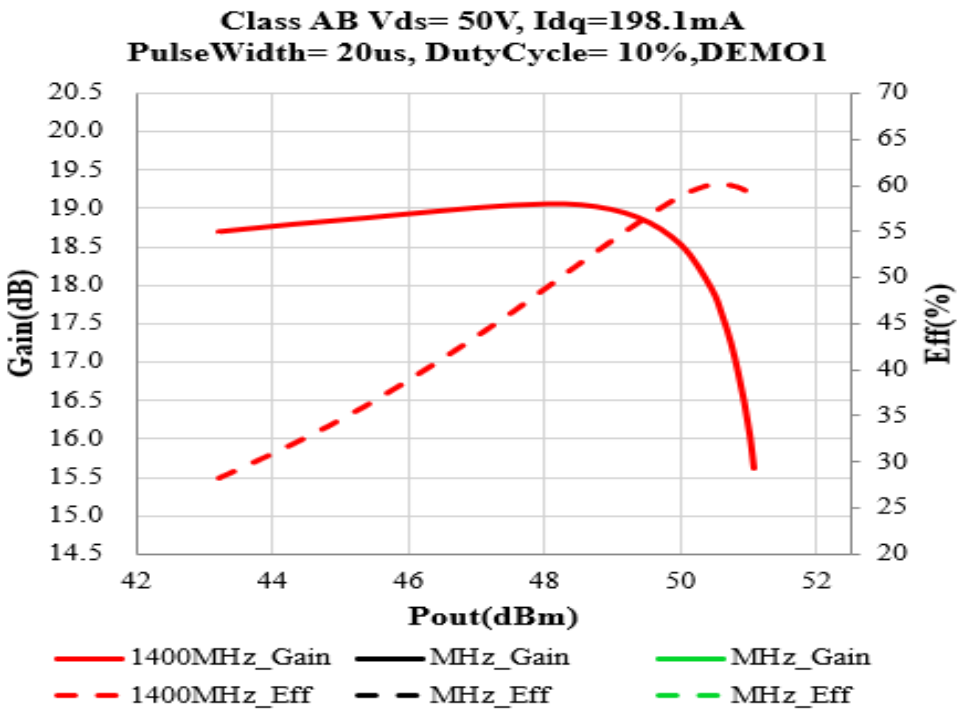
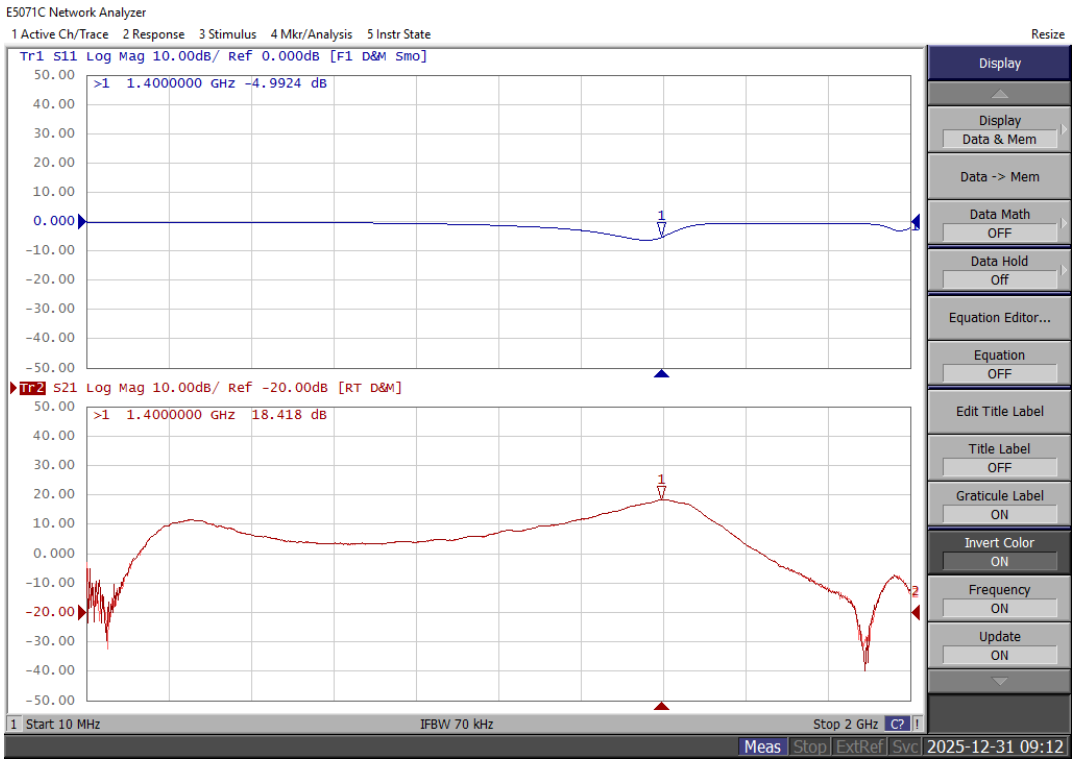
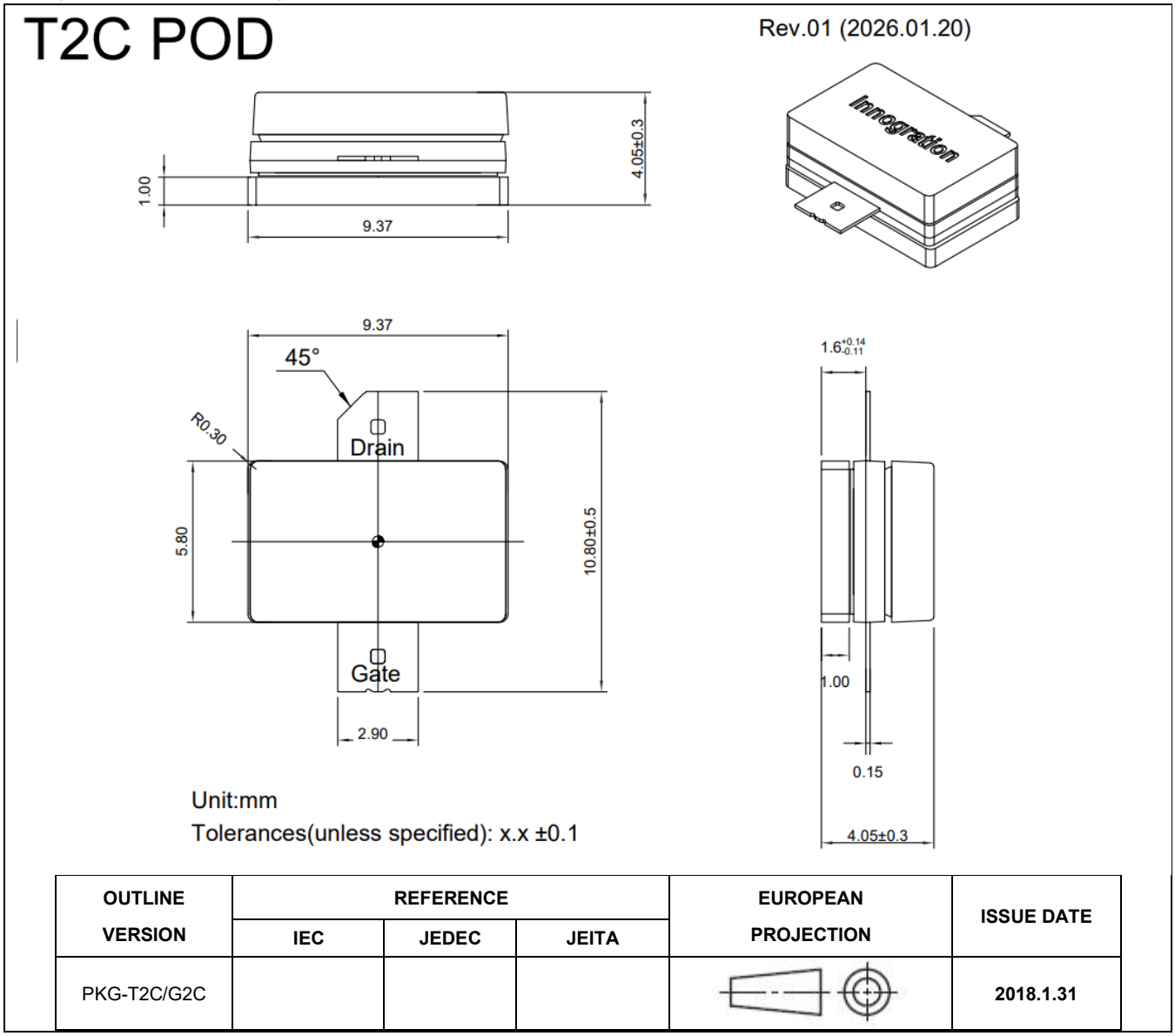


Figure 5.Network analyzer output S11/S21



Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-T2C/G2C					2018.1.31

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/12/31	Rev 1.0	Preliminary Datasheet

Application data based on HZH-25-20

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