



80W,28V Sub-1.5GHz RF LDMOS Transistor

Description

The ITGH09080T2C is a 80-watt, high performance, LDMOS transistor, designed for any general applications at frequencies up to 1.5GHz. **It is based on air cavity plastic package named as T2C with outline highly compatible as TO270 from other suppliers**



- Typical 915MHz Class AB RF Performance (On Innogrator fixture with device soldered).

V_{ds}=28V,I_{dq}=100mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
915	48.76	75.2	73.7	19.35	49.53	89.8	76.6

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- RF power amplifiers for CW applications
- Industrial, scientific and medical applications
- Broadcast transmitter applications
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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+65	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+28	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, DC test, device soldered on heatsink directly	R _{θJC}	0.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Voltage V _{GS} =0, I _{DS} =100uA	V _{(BR)DSS}		65		V
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Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28V, V_{GS} = 0V$)	I_{loss}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 11V, V_{DS} = 0V$)	I_{loss}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28V, I_D = 600\mu A$)	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ($V_{DD} = 28V, I_D = 400mA$, Measured in Functional Test)	$V_{GS(Q)}$	—	2.5	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 28Vdc, I_{DQ} = 400mA, f = 915MHz$

VSWR 10:1 at 80W pulse CW Output Power	No Device Degradation
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915MHz application board

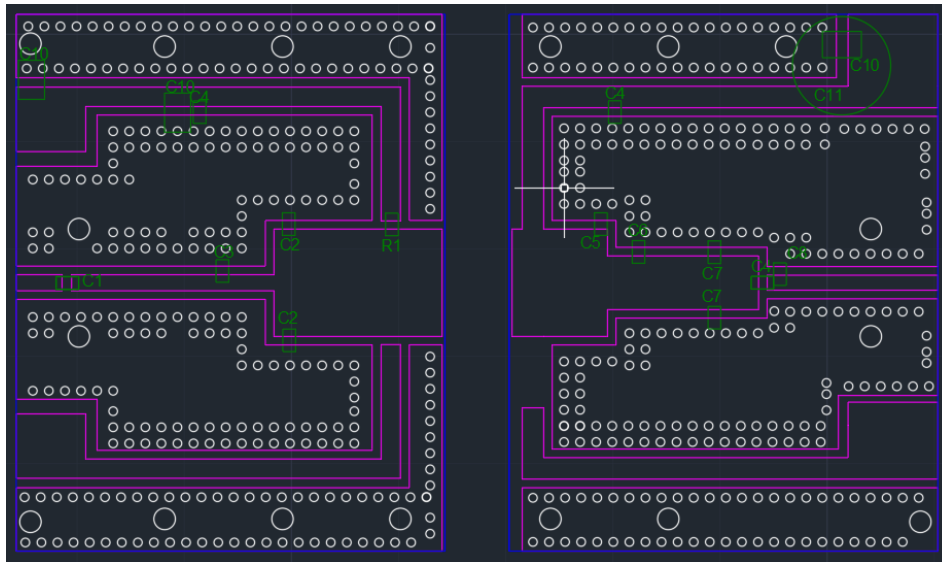


Figure 2. Test Circuit Component Layout, 30mils RO4350B

Note:

Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
C1	3.9pF	1
C2	6.2pF	2
R1	10 ohm	2
C11	470uF	1
C3	2pF	1
C4	100pF	3
C6	2pF	1
C7	3.3pF	2
C10	10uF	3
C5	8.2pF	1
C8	3.9pF	1

TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output

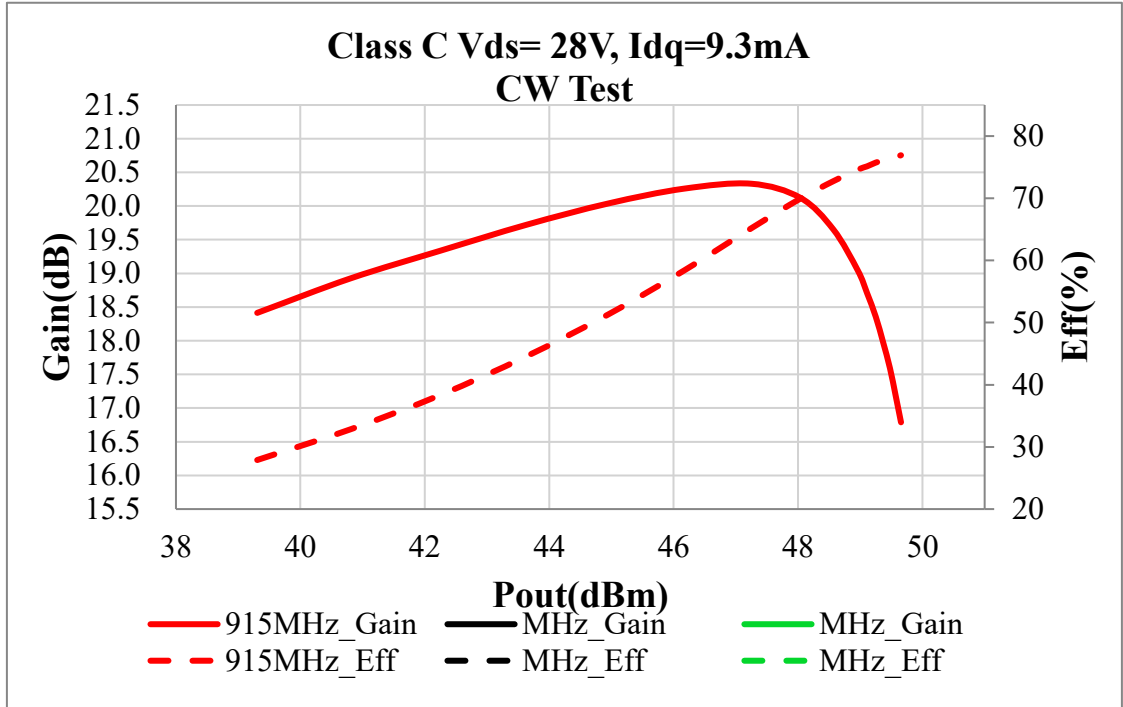
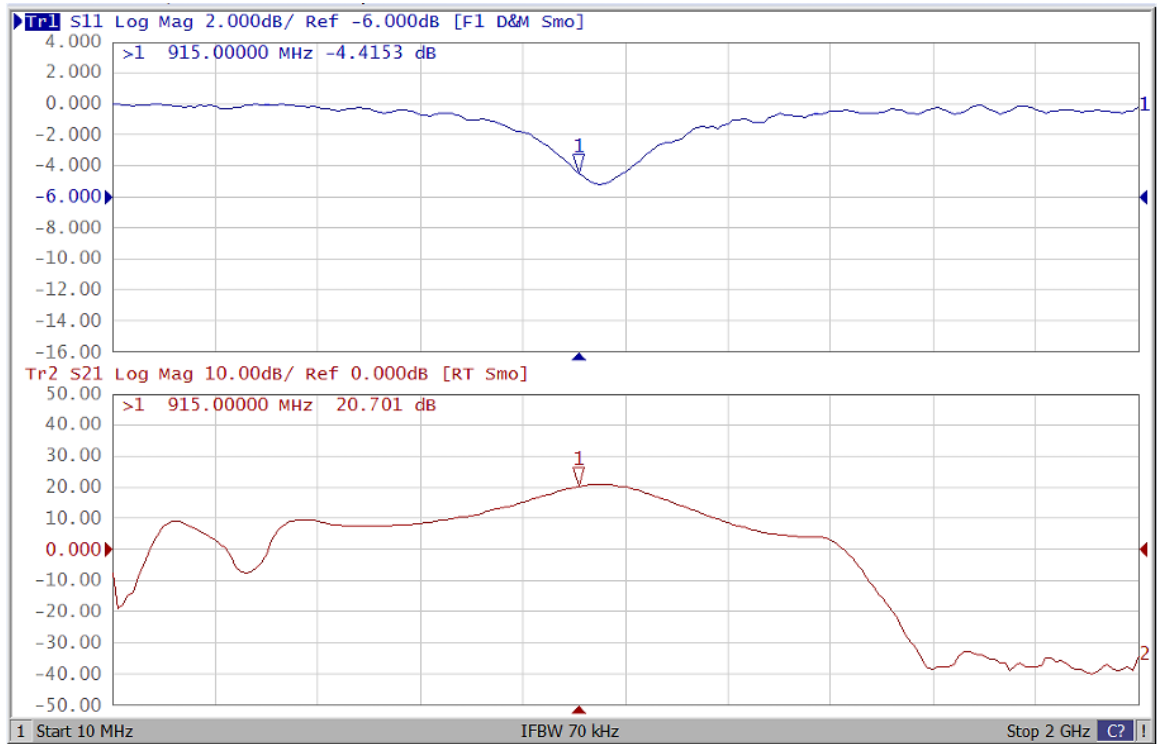


Figure 4. Network analyzer output S11/S21



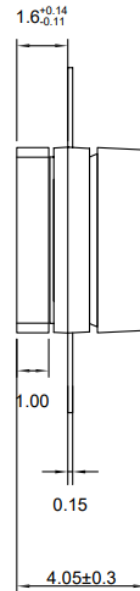
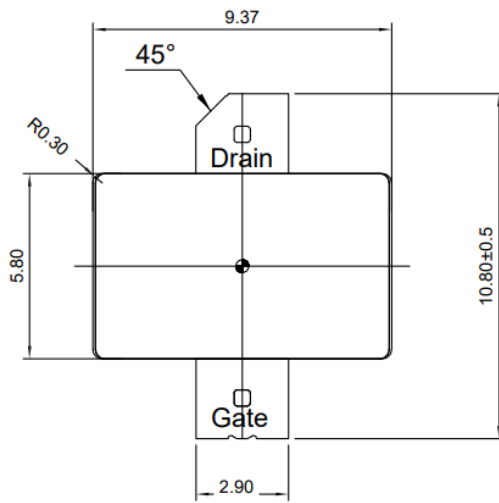
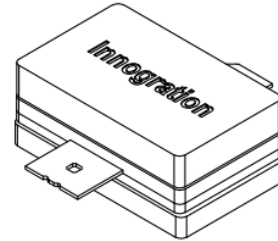
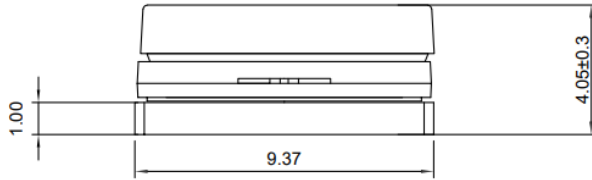


Package Outline

Flanged ceramic package; 2 leads

T2C POD

Rev.01 (2026.01.20)



Unit:mm

Tolerances(unless specified): x.x ±0.1

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-T2C					2018.1.31



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/12/29	Rev 1.0	Preliminary Datasheet

Application data based on ZXY-25-16

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